

Two-Stage CMOS Operational Amplifier  
Design with SKY130

Warrick Lo

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# 1. Introduction

The operational amplifier (often called “op-amp”) is device that amplifies a differential input into a single-ended output voltage. This project and report will focus on the voltage-feedback op-amp, which amplifies the voltage difference between the inputs.

The output voltage of the op-amp can be given by

$$V_{\text{out}} = A_v (V_+ - V_-), \quad (1.1)$$

where  $V_+$  is the non-inverting input,  $V_-$  is the inverting input, and  $A_v$  is the open-loop gain of the op-amp. An ideal op-amp will have many characteristics, such as infinite open-loop gain  $A_v$ , infinite input resistance  $R_{\text{in}}$ , zero output resistance  $R_{\text{out}}$ , infinite bandwidth, zero phase shift, and infinite slew rate. Of course, these cannot be physically realised and are limited by real world constraints among other limitations. Operational amplifier designs must therefore carefully balance their characteristics and make trade-offs to achieve their desired performance metrics.

In this project, we will design and simulate a two-stage complementary MOSFET (CMOS) operational amplifier, implemented in SkyWater’s SKY130 open source 130 nm process development kit (PDK).<sup>1</sup> This report will first outline the topology used and design objectives, then go over the design process using open source software tools, and finally an analysis of performance results.

## 1.1. Design Topology

We will employ a two-stage amplifier design. The first stage is a high-gain differential-to-differential amplifier, and the second stage is a high-swing differential-to-single-ended amplifier. Since we have a differential voltage in between the two stages, a common-mode feedback circuit is also needed to regulate the DC voltage.

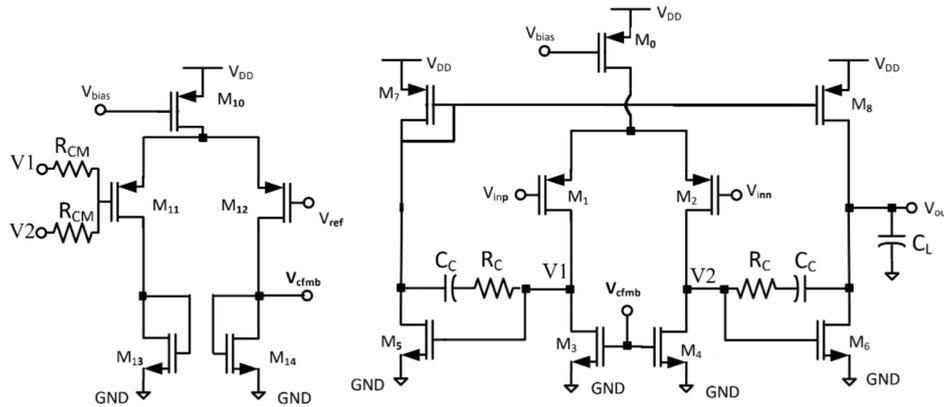


Figure 1.1. Design topology of the operational amplifier.

<sup>1</sup><https://github.com/google/skywater-pdk>.

## 1.2. Design Objectives

Parameter	Symbol	Specification
Supply voltage	$V_{DD}$	1.8 V
Reference voltage	$V_{SS}$	0 V
Input common-mode voltage	$V_{in(CM)}$	0.9 V
Output common-mode voltage	$V_{out(CM)}$	0.9 V
Power consumption	$P$	$\leq 0.4$ mW
Differential output swing	$\Delta V_{out}$	$\geq 1.2$ V
Low-frequency differential gain	$A_v$	$\geq 46$ dB
Small-signal unity gain frequency	$f_u$	$\geq 60$ MHz
Phase margin	$\phi_m$	$\geq 60^\circ$ & $\leq 90^\circ$
Slew rate	$S$	$\geq 20$ V/ $\mu$ s

**Table 1.1.** Project design objectives.

## 2. Design Process

## 3. Results

### 3.1. Performance Overview

Parameter	Symbol	Specification	Achieved
Supply voltage	$V_{DD}$	1.8 V	1.8 V
Reference voltage	$V_{SS}$	0 V	0 V
Input common-mode voltage	$V_{in(CM)}$	0.9 V	0.9 V
Output common-mode voltage	$V_{out(CM)}$	0.9 V	0.898 V
Power consumption	$P$	$\leq 0.4$ mW	282.2 $\mu$ W
Differential output swing	$\Delta V_{out}$	$\geq 1.2$ V	?
Low-frequency differential gain	$A_v$	$\geq 46$ dB	50.48 dB
Small-signal unity gain frequency	$f_u$	$\geq 60$ MHz	66.2 MHz
Phase margin	$\phi_m$	$\geq 60^\circ$ & $\leq 90^\circ$	75.2 $^\circ$
Slew rate	$S$	$\geq 20$ V/ $\mu$ s	75.8 V/ $\mu$ s

**Table 3.1.** Performance results of the final design.

## 4. Conclusion